Amendments to the Claims

A complete list of pending claims follows:

1. (Previously Amended) An information handling system, comprising:

a plurality of processors coupled to a processor bus; and

a memory;

wherein each of the processors is operable to enter an interrupt mode and wherein a uniquely addressable semaphore in memory is associated with each processor and indicates whether the associated processor has exited the interrupt mode.

2. (Original) The information handling system of claim 1, wherein each of the semaphores is stored in a memory location that is offset from a base memory location by a unique offset indicator.

3. (Currently Amended) The information handling system of claim 1, wherein each processor is operable to access the semaphores associated with the other processors of the information handling system.

4. (Original) The information handling system of claim 1, wherein each processor is operable to access the semaphores associated with the processors of the information handling system on a non-exclusive basis.

5. (Original) The information handling system of claim 1, wherein the memory location associated with the storage of the semaphores associated with the processors of the

information handling system is memory space dedicated to storing data associated with the entry of the processors into interrupt mode.

6. (Original) The information handling system of claim 1, wherein the interrupt mode is system management interrupt mode.

7. (Currently Amended) The information handling system of claim 1,

wherein the interrupt mode is system management interrupt mode;

wherein the semaphore associated with a processor is stored in a memory location that is offset from a base memory location by a unique offset indicator associated with the processor; and

wherein each processor is operable to access the semaphores associated with the other processors of the information handling system on a non-exclusive basis.

8. (Currently Amended) A method for processing an interrupt in a multiple processor computer system, comprising the steps of:

for each processor, entering interrupt mode;

for each processor, setting a semaphore associated with the processor to indicate that the processor is in interrupt mode, wherein a uniquely addressable semaphore in a memory of the computer system is associated with each processor;

for the interrupt handling processor, performing the tasks necessary to resolve the interrupt and negating the semaphores associated with the non-interrupt handling processors of

the computer system, wherein the negation of the semaphores indicates that the non-interrupt handling processors have exited the interrupt mode; and

for each non-interrupt handling ~~processors~~ processor, exiting interrupt mode following the negation of the semaphore associated with the processor.

9. (Original) The method for processing an interrupt in a multiple processor computer system of claim 8, wherein the step of setting a semaphore for each processor comprises the step of setting the semaphore for each processor on a non-exclusive basis.

10. (Original) The method for processing an interrupt in a multiple processor computer system of claim 8, wherein the step of negating the semaphores of the non-interrupt handling processors of the computer system comprises the step of negating the semaphores of the non-interrupt handling processors of the computer system on a non-exclusive basis.

11. (Original) The method for processing an interrupt in a multiple processor computer system of claim 8, wherein the interrupt is a system management interrupt.

12. (Original) The method for processing an interrupt in a multiple processor computer system of claim 8, wherein each of the semaphores are stored in a memory location that is offset from a base memory location by a unique offset indicator.

13. (Original) The method for processing an interrupt in a multiple processor computer system of claim 8,

wherein the step of setting a semaphore for each processor comprises the step of setting the semaphore for each processor on a non-exclusive basis;

wherein the step of negating the semaphores of the non-interrupt handling processors of the computer system comprises the step of negating the semaphores of the non-interrupt handling processors of the computer system on a non-exclusive basis; and

wherein each of the semaphores are stored in a memory location that is offset from a base memory location by a unique offset indicator.

14. (Original) The method for processing an interrupt in a multiple processor computer system of claim 8,

wherein the interrupt is a system management interrupt;

wherein the step of setting a semaphore for each processor comprises the step of setting the semaphore for each processor on a non-exclusive basis;

wherein the step of negating the semaphores of the non-interrupt handling processors of the computer system comprises the step of negating the semaphores of the non-interrupt handling processors of the computer system on a non-exclusive basis; and

wherein each of the semaphores is stored in a memory location that is offset from a base memory location by a unique offset indicator.

15. (Previously Amended) A computer system, comprising:

a plurality of processors;

a memory;

wherein the architecture of the processors and the memory is a non-uniform memory access architecture; and

wherein each of the processors is operable to enter an interrupt mode and wherein a uniquely addressable semaphore in memory is associated with each processor and indicates whether the associated processor has exited the interrupt mode.

16. (Original) The computer system of claim 15, wherein the interrupt mode is associated with a system management interrupt.

17. (Original) The computer system of claim 16, wherein each of the semaphores is stored in a memory location that is offset from a base memory location by a unique offset indicator.

18. (Original) The computer system of claim 17, wherein the memory location associated with the storage of the semaphores is memory space dedicated to storing data associated with the entry of the processors into interrupt mode.

19. (Original) The computer system of claim 16, wherein the semaphores may be accessed by each of the processors on a non-exclusive basis.

20. (Original) The computer system of claim 16,

wherein the semaphores may be accessed by each of the processors on a non-exclusive basis; and

wherein each of the semaphores is stored in a memory location that is offset from a base memory location by a unique offset indicator.